Junction profiles of sub keV ion implantation for deep sub-quarter micron devices

Junction Profiles of Sub keV Ion Implantation for Deep Sub-quarter Micron Devices

Amir Al-Bayati, Sanjeev Tandon, Roisin Doherty, Adrian Murrell, Dennis Wagner, Majeed Foad and Babak Adibi,
Applied Materials, Implant Division, 3050 Bowers Ave., Santa Clara, CA, 95054, USA.

Rimvydas Mickevicius, Victor Meniailenko, and Simeon Simeonov
ISE Integrated Systems Engineering AG, 111 Market st, suite 800, San Jose, CA 95113 USA

Amitabh Jain
Silicon Technology Research, Texas Instruments, MS3701, 13570 N Central Expressway, Dallas, TX, 75243, USA.

David Sing, Clarence Ferguson, Robert Murto, and Larry Larson.
International Sematech, Front End Processing Division, 2706 Montopolis Drive, Austin, TX, 78741, USA.

Abstract- **Ultra shallow junctions <500 Å with steep profiles <8nm/decade are required for device technologies ≤0.13 μm as outlined by the recent ITRS Roadmap. For a p^+/n junction such profiles can be obtained using sub-keV B ion implantation since both the projected range and more importantly the transient enhanced diffusion are significantly reduced at lower energies. State-of-the-art high current implanters utilize deceleration mode typically for sub 1 keV implantation in order to increase the beam current and production wafer throughput. Such a mode contains a very low level of energy contamination. This level is measured for sub keV B implants in the Quantum Leap and factors affecting the level of contamination are studied. Spike and soak annealing reduces the effect of the energy contamination on junction profile and depth. The effect of energy contamination on device performance such as L_{eff}, V_T and I_{DSAT} is simulated using ISE TCAD.**

I. Introduction

Deep sub quarter micron devices require junctions less than 500 Å deep in order to reduce the short channel effects [1]. Lowering the implant energy to 1 keV and below for B not only reduces the projected range but more importantly decreases the transient enhanced diffusion (TED) [2], which is caused by point defects produced during the implant. A lower concentration of point defects, closer to the surface, are produced by low energy implants, hence lower TED. However, lowering the ion energy to keV and below reduces the available beam current for implantation due to the space charge blow-up effect, which increases with decreasing ion energy (blow up is proportional to $(I/V^{3/2})^{1/2}$.where V stands for ion energy and I for positive ion beam current). Improvements to the current of drift beams at low energies can be obtained through design optimization of the extraction optics and beamline. Recent work in our lab showed that 2x improvement to the beam current down to 1 keV have been obtained using a more efficient extraction optics [3]. Further increases in beam current at low energies, particularly <1 keV, can be obtained through the use of a deceleration mode. In this mode the ion beam is transported from the source at relatively higher energies than the implant energy and decelerated to the implant energy at a short distance before the wafer. Such a mode could introduce "energy contamination" in the implant, in which some percentage of the ions are implanted with their initial energies before the deceleration. Energy contamination could affect the shape of the implant profile, junction depth and metallurgical junction in the CMOS channel. Yasunaga et al.., showed that devices can tolerate energy contamination up to 3% so long as the level of contamination is repeatable to +/-10% [4].

The mechanism by which energy contamination is formed is discussed as follows. The primary ions (A^+) before deceleration lose their charge, through a charge exchange collision, to the residual gas molecules (B) through the following reaction:

$$A^+ (fast) + B (slow) \rightarrow A (fast) + B^+ (slow) \qquad (1)$$

After collision the dopant atoms keep their initial energy and implant the wafer at this energy, yielding a deeper dopant profile. On the other hand, dopant ions that did not lose their charge lose energy in the deceleration stage and implant the wafer with a lower energy than the initial energy, yielding a shallower profile. The deeper profile distorts the shallower profile and the level of distortion depends to a large extent on the magnitude of initial energy and percentage of energy contamination. The percentage of contamination is proportional to the pressure, charge exchange cross section, length of travel (before the deceleration lens and in line of site with the wafer) [5]. Pressure variations can result in changes in the percentage of energy contamination and, therefore, it is important to keep pressure variations to a minimum level.

The objectives of this paper are to study the effects of energy contamination on junction depth and profile before and after annealing, and on device performance. We have investigated the effect of initial energy and deceleration ratio on the percentage of contamination in low energy beams down to 200 eV. We have also studied the effect of soak and spike annealing on the junction formed. The effect of energy contamination on device performance is studied using ISE (Integrated System Engineering) TCAD software.

0-7803-6462-7/00/$10.00 © 2000 IEEE

II. Experimental

Low energy B implants and annealing have been performed on the Applied Materials Quantum Leap implanter [3] and Radiance RTP (Rapid Thermal Processing), respectively. Wafers have been implanted with B in the energy range of 0.2 to 1 keV using the deceleration mode and 0.5-1 keV using the drift mode. For both modes a dose in the range of $2x10^{14}$ to $1x10^{15}$ cm^{-2} has been used. For the deceleration mode the range of initial acceleration energy investigated is 1-5 kV. Prior to B implants all wafers are pre-amorphized using 5 keV Ge to a dose of $1x10^{15}$ cm^{-2}. Following B implants wafers are either not annealed, soak annealed at 1050 °C for 10 sec or spike annealed to 1050 C using a ramp rate of 250 °C/sec. SIMS analysis is used to determine the effect of energy contamination on the dopant profile.

III Results and Discussion

A. *As-implanted*

Fig 1 shows SIMS comparisons between drift and decelerated profiles of different initial energies and for the same final energy of 1 keV. The decelerated profile in Fig. 1 A is obtained using an initial energy of 5 keV. The figure shows a clear broadening to the profile by the energy contamination from the 5 keV B. The percentage of this contamination

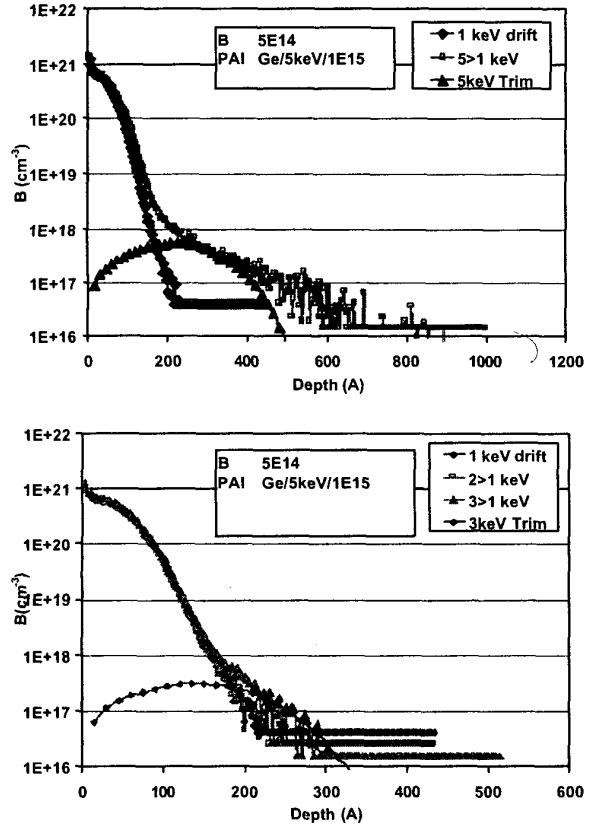

Fig. 1. SIMS comparison between drift and decelerated implants for the same final energy of 1 keV. A (top) initial energy= 5kV; B(bottom) initial energies =3 and 2kV.

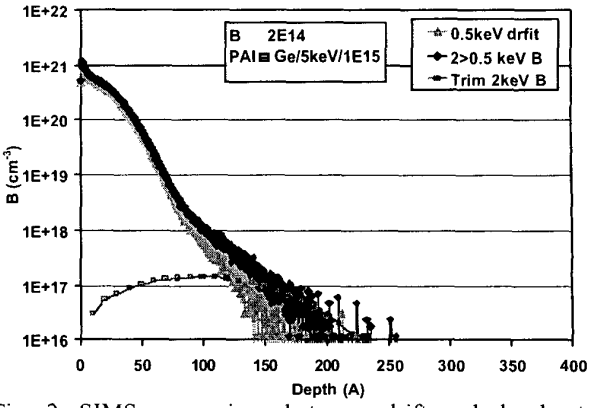

Fig. 2. SIMS comparison between drift and decelerated implants for the same final energy of 0.5 keV. Initial energy=2kV.

is estimated by fitting a TRIM simulation of 5 keV B profile in the deeper portion of the SIMS profile as shown in the figure. As the initial energy drops to 3 and 2 kV the level of energy contamination is significantly reduced. Fig. 1 B shows that the profile of decelerated beam from 2 kV is almost indistinguishable from the drift profile. This is partly because the profile of 2 keV B is closer to that of the 1 keV profile. Fig. 2 shows as the final energy is dropped to 0.5 keV, contamination from 2 kV B is visible, but still insignificant.

The above results indicated that both the initial energy and deceleration ratio (initial/final energy) affect the % (percentage) of contamination. To quantify their effects we calculated the % of contamination versus initial energy and deceleration ratio for the final energies of interest (0.2-1keV). The % of contamination is calculated from the TRIM fit to the deeper profile divided by the nominal B dose times 100. Fig. 3 shows that the percentage of energy contamination increases with increasing energy as expected and that the lowest percentage is obtained at initial energy below 5 kV. On the other hand, Fig. 4 shows a weak dependency on the deceleration ratio. These results indicate that it is important to reduce the initial energy to 3 keV and below for sub keV B in order to reduce the percentage of contamination.

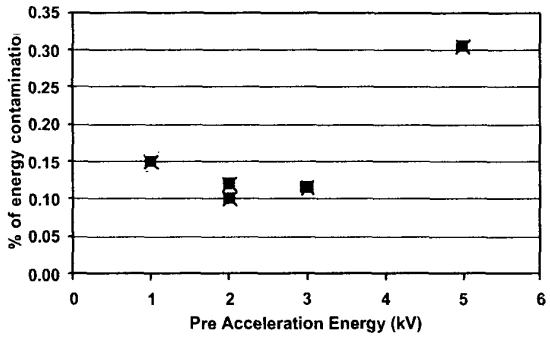

Fig. 3. Percentage of energy contamination versus initial acceleration energy.

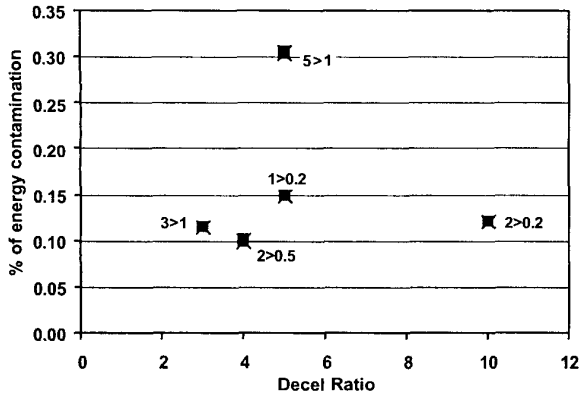

Fig. 4. Percentage of contamination versus deceleration ratio.

B. Annealed

The effect of spike and soak annealing on the dopant profile and junction formed by drift and decelerated implants are shown in Fig. 5. The implant dose for these profiles is $1x10^{15}$ cm^{-2} and it is 2x higher than that shown in Fig. 1, but the effect of energy contamination on the as-implanted profile is similar. After annealing the drift and decelerated profiles look very similar in particular at dopant concentrations above $1x10^{17}$ cm^{-3}. These results indicate that the effects of energy contamination on the dopant profile and junction depth are significantly reduced after annealing, and that decelerated mode can be used for producing ultra shallow junctions with X_j<450 Å. Decelerated mode gives significant improvement to beam current over drift mode and hence higher productivity. For example decelerated beam current from 3 keV to 1 keV is 3x higher than drift beam current of 1 keV.

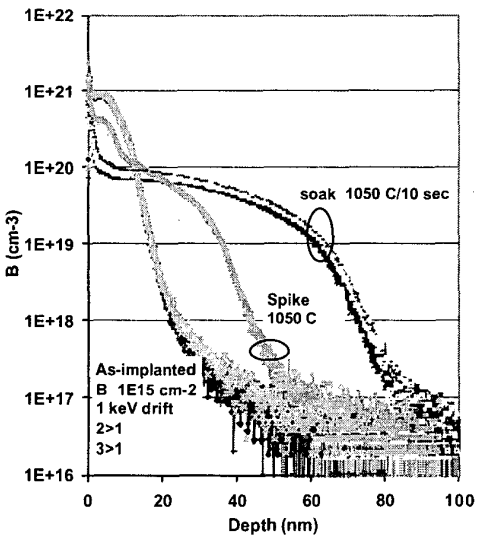

Fig. 5. As-implanted, spike and soaked annealed profiles for a final energy of 1 keV. Drift vs decelerated beams from 3 and 2 kV.

C. TCAD Simulation

The effect of energy contamination on device performance is studied using ISE TCAD simulation software. A PMOS transistor with L_{poly} of 130 nm is used for this study as shown in Fig. 6. The source and drain extensions are formed using 0.5 keV B to a dose of $1x10^{15}$ (no pre-amorphization implant) followed by spike annealing to 1050 °C (250 °C/s up, 90 °C/s down) - this procedure is termed baseline. The effect of energy contamination is studied by implanting a known amount of 2 keV B on top of the baseline implant. This amount of energy contamination is varied from 0.05 to 5%. Fig 7 shows the vertical SDE profile following B implant and spike annealing for different % of energy contamination. The simulations were performed using process simulator DIOS [6]. The results show a negligible increase to the junction at $1x10^{18}$ cm^{-3} for contamination levels <1%, and a small increase in the junction depth even at 5% (ΔX_j= 40 Å). The simulation results agree with the experimental results shown in Fig. 5, as far as th eeffect of contamination on the profile.

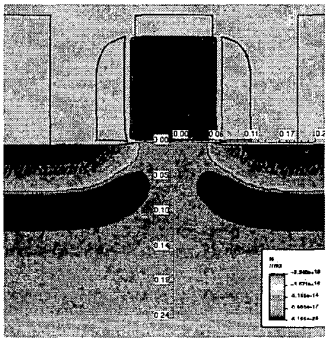

Fig. 6. PMOS layout with L_{poly}=130 nm used for simulating the effect of energy contamination in B implants used for the source drain extensions.

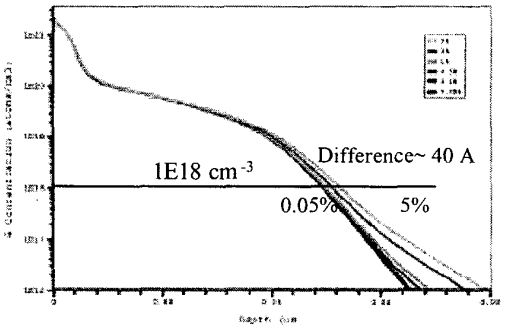

Fig. 7. Simulated B dopant profiles of 0.5 keV B $1x10^{15}$ and spike annealed to 1050 °C for different % of 2 keV B contamination.

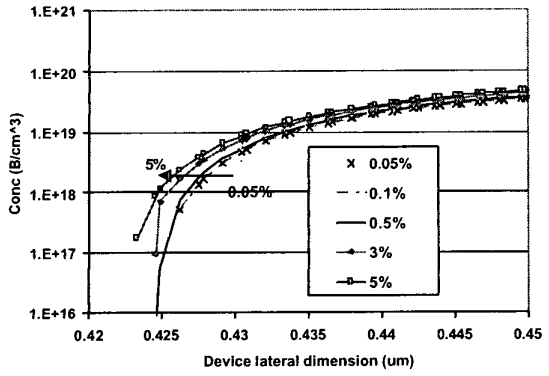

Fig. 8. Dopant profiles along the device channel for B implants with different % of energy contamination.

The effect of energy contamination on the lateral profile of SDE is also studied and the results are shown in Fig 8. For actual levels of contamination in the Quantum Leap, i.e. <0.15% the lateral junction changes by <2.5 Å; for 5% contamination the lateral junction changes by 25 Å. Fig. 9 shows these changes on the effective channel length L_{eff}.

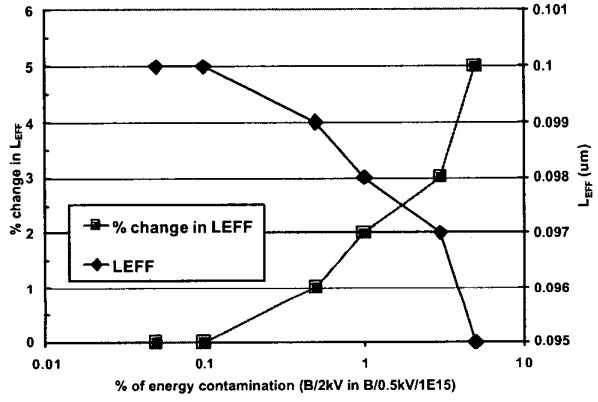

Fig. 9. Changes to effective channel length (L_{eff}) vs % of energy contamination

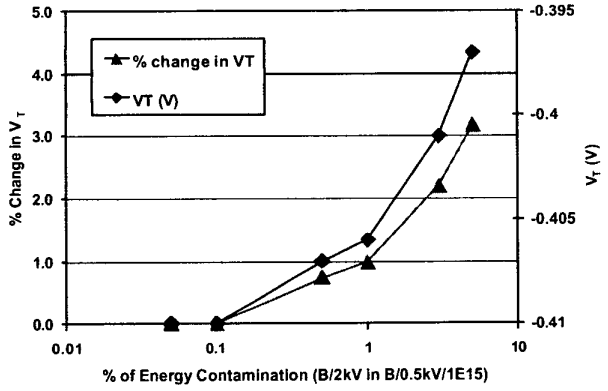

Fig. 10. Changes to V_T vs % of energy contamination.

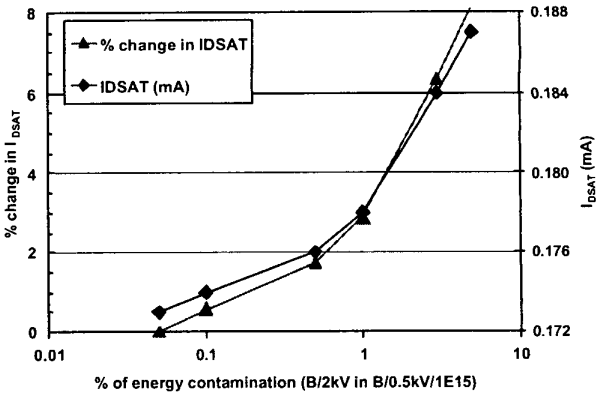

Fig. 11. Changes to drive current (I_{dsat}) vs % of energy contamination.

So for contamination <0.15% L_{eff} changes only by 0.5% or 5 Å –this is a much lower variation than typical CD variation in device manufacturing of +/- 5-10% of L_{poly} (i.e. +/- 50-100 Å).

Figs 10 and 11 show the effect of energy contamination on threshold voltage and drive current. Again, these figures show small percentage change to V_T and I_{DSAT} due to actual level of contamination in the Quantum Leap. The electrical characteristics of the device were simulated using mesh generator MDRAW [7] and device simulator DIOS [6]

IV. CONCLUSIONS

Actual percentage of energy contamination in the Quantum Leap is very low (<0.15%). The effect of energy contamination on the junction is almost eliminated after spike and soak annealing. ISE TCAD device simulation shows that contamination levels <0.15% yields negligible effect on device performance and that devices may tolerate even a higher level of contamination up to a few percent in agreement with [4].

REFERENCES

[1] International Technology Roadmap for Semiconductor, 1999
[2] Aditya Agarwal, Hans-J Gossmann, and Anthony T. Fiory, Mat. Res. Soc. Symp. Proc, V568, p19, 1999.
[3] Adrian Murrell et al, these proceedings
[4] T. Yasunaga, Matsuda, S. Shishiguchi, and S. Saito, Proceeding of IIT1998, p18.
[5] K. Leyland , D.G. Armour, G. Carter, and J.H. Freeman, Inst. Phys. Conf. Ser. No. 38, 175 (1978)
[6] DIOS Manual, Rel. 6.1, Vol. 3, Zurich Switzerland, ISE Integrated Systems Engineering AG, 2000. (see also www.ise.com)
[7] MDRAW Manual, Rel. 6.1, Vol. , Zurich Switzerland, ISE Integrated Systems Engineering AG, 2000. (see also www.ise.com)